REMARKS

Amended Claims

Claims 15, 19, 23 and 27 are amended herein into independent form, including all of the limitations of the base claim and any intervening claims, to overcome the Examiner's objection. Applicant contends that no new matter has been added by these amendments.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-12 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses the rejection. Applicant maintains that claims 1-12 contain subject matter that was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, how to make and/or use the claimed invention.

In rejecting claims 1-12, the Examiner stated that "[t]he limitations comprising a computer system and CPU are not described in the specification such that one skilled in the art would be able to make or use the components as claimed."

Applicant respectfully maintains that the computer system and CPU recited in claims 1-12 are detailed in the Application, at least, by Figure 5 and page 4, lines 10-12 and page 6, line 22 to page 7, line 24. In particular, Applicant notes that page 4, lines 10-12, recites in part, "[i]n one aspect, the system may include a central processing unit (CPU), and a memory device coupled to the processor that includes an array having memory cells . . ." and page 6, line 22 to page 7, line 2 recites, in part, "[t]he computer system 100 includes a processor 102 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 102 includes a processor bus 104 that normally includes an address bus, a control bus, and a data bus. The processor bus 104 is coupled to a memory controller 106, which is, in turn, coupled to a number of other components. The processor 102 is also typically coupled through the processor bus 104 to a cache memory 107, which is usually a static random access memory ("SRAM") device." Applicant maintains that the terms "computer system" or "CPU" and the description of Figure 5 and page 4, lines 10-12 and page 6, line 22 to page 7, line 2 would be interpreted by one of ordinary skill in the art as disclosing and enabling a CPU and a computer system.

Applicant contends that relevant features of claims 1-12 have been described in the

specification to allow one skilled in the art to practice the invention. Applicant therefore maintains that claims 1-12 and the terms "computer system" or "CPU" are considered to be described and enabled by the specification. The Applicant therefore requests that the rejection of claims 1-12 under 35 U.S.C. § 112, first paragraph, be withdrawn in that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 102

Claims 13, 14, 16 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kolodny et al. (U.S. Patent No. 4,785,199). Applicant respectfully traverses this rejection and submits that claims 13, 14, 16 and 17 are allowable for at least the following reasons.

Applicant respectfully maintains that Kolodny et al. discloses a programmable CMOS logic gate structure, having both a P-FET and an N-FET device, and does not disclose a floating gate memory cell. Applicant further maintains that Kolodny et al. does not disclose a floating gate memory cell structure containing a first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance. *See, e.g.*, Kolodny et al., Figs. 1 and 3, Abstract, column 2, line 53 to column 3, line 37. The Applicant therefore respectfully maintains that Kolodny et al. does not teach or disclose a memory cell having a floating gate structure that is spaced apart from the source/drain/channel regions in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second section by a second distance, wherein the first distance is less than the second distance.

Claim 13 recites, in part, "an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance." As stated above, Kolodny et al. does not teach or disclose a memory cell having a first and second adjacent field effect transistors (FETs) having a common floating gate. Therefore, Kolodny et al. does not teach or disclose all elements of claim 13.

Claim 14 recites, in part, "an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance." As stated above, Kolodny et al. does not teach or disclose a memory cell having a first and second adjacent field effect transistors (FETs) having a common floating gate. Therefore, Kolodny et al. does not teach or disclose all elements of claim 14.

Applicant respectfully contends that claims 13 and 14 have been shown to be patentably distinct from the cited reference. As claims 16 and 17 depend directly or indirectly from independent claim 13, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 13, 14, 16 and 17.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 9-12, 18, 22, 25, 26 and 28-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama (U.S. Patent No. 4,630,085). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant submits that claims 1, 9-12, 18, 22, 25, 26 and 28-32 are allowable for the following reasons.

Applicant respectfully maintains that Koyama discloses a single floating gate FET EPROM gate structure, wherein the floating gate is uniformly spaced from the source and drain and where the source and drain regions have different doping concentrations. *See, e.g.*, Koyama, Figs. 4 and 5, Abstract, column 6, line 37 to column 8, line 5. The Applicant therefore respectfully maintains that Koyama does not teach or suggest a floating gate memory cell structure containing a first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance.

Claim 1 recites, in part, "an array having memory cells arranged in rows and columns for storing a desired logic state, each cell including a first columnar structure and a spaced apart

second columnar structure having a floating gate structure interposed between the first columnar structure and the second columnar structure and spaced apart from the first and second structures, the floating gate being positioned closer to a selected one of the first and second structures." As stated above, Koyama does not teach or suggest such an array of memory cells, each cell including a first and second adjacent field effect transistors (FETs) having a common floating gate, the floating gate being positioned closer to a selected one of the first and second FETs. Therefore, Koyama does not teach or suggest all elements of claim 1.

Claim 22 recites, in part, "forming a gate structure between the first structure and the second structure; and interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure, the floating gate structure being positioned closer to selected one of the first structure and the second structure." As stated above, Kolodny et al. does not teach or suggest a method of forming a memory device having a plurality of interconnected memory cells, each cell comprising a first and second adjacent field effect transistors (FETs) having a common floating gate, the floating gate being positioned closer to a selected one of the first and second FETs. Therefore, Kolodny et al. does not teach or suggest all elements of claim 22.

Applicant respectfully contends that claims 1 and 22 have been shown to be patentably distinct from the cited reference. As claims 9-12, 18, 25, 26 and 28-32 depend from and further define claims 1 and 22, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 9-12, 18, 22, 25, 26 and 28-32.

Allowable Subject Matter

Claims 15, 19-21, 23, 24 and 27 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant has amended claims 15, 19, 23 and 27 as suggested by the Examiner. As claims 20-21 and 24 depend from and further define claims 19 and 23, respectively, they are also considered to be in condition for allowance. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claims 15, 19-21, 23, 24 and 27.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 5/19/05

Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250